library IEEE;

use IEEE.std\_logic\_1164.all;

entity ula\_1b\_tb is

end ula\_1b\_tb;

architecture arch\_ula\_1b of ula\_1b\_tb is

component ula\_1b

port (

a, b, less, binvert, carryin, operation: in std\_logic;

resultado, set, overflow: out std\_logic;

);

end component;

signal a : std\_logic;

signal b : std\_logic;

signal less: std\_logic;

signal binvert : std\_logic;

signal carryin : std\_logic;

signal operation : std\_logic;

signal resultado : std\_logic;

signal set : std\_logic;

signal overflow : std\_logic;

begin

uut : ula\_1b port map(

a => a;

b => b;

less => less;

binvert => binvert;

carryin => carryin;

operation => operation;

resultado => resultado;

set => set;

overflow => overflow;);

tb : process

begin

wait for 10 ns;

a <= ‘0’;

b <= ‘0’;

less <= ‘0’;

binvert <= ‘0’t;

carryin <= ‘0’;

operation <= ‘0’;

wait for 10 ns;

end process

end arch\_ula\_1b